Good quality Al/SiN_x:H/InP metal-insulator-semiconductor devices obtained with electron cyclotron resonance plasma method

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We have obtained Al/SiN_x:H/InP metal-insulator-semiconductor devices depositing SiN_x:H thin films by the electron cyclotron resonance plasma method at 200 °C. The electrical properties of the structures were analyzed according to capacitance–voltage and deep level transient spectroscopy measurements. We deduce an inverse correlation between the insulator composition—the N/Si ratio—and the density of interface traps: those films with the maximum N/Si ratio (1.49) produce devices with the minimum trap density—2×10^{12} cm^{-2} eV^{-1} at 0.42 eV. above the midgap. We explain the influence of film composition on the interface trap density in terms of a substitution of phosphorous vacancies at the InP surface, V_p, by N atoms coming from the insulator, N_{Vp}. The values obtained in our research for the interface trap distribution were similar to other published results for devices that use chemical and/or physical passivation processes of the InP surface prior to the deposition of the insulator. © *1998 American Institute of Physics.* [S0021-8979(98)08501-6]

I. INTRODUCTION

There is a growing interest in the deposition of insulator thin films by the electron cyclotron resonance (ECR) plasma method, to be used in metal-insulator-semiconductor field effect transistor (MISFET) device technology.[1] This plasma process has proved to be highly suitable to obtain insulator films with good physical properties at very low substrate temperature (200 °C or below). Good quality films of SiN_x:H, [2] SiO_2,[3] and SiO_xN_y[4] have been obtained with this technique. Recently, films of SiN_x:H deposited by ECR have been used in metal-insulator-semiconductor (MIS) devices with different III–V semiconductors like GaAs,[1] InGaAs,[5] and InP.[6] In all the devices, prior to the deposition of the insulator, it was necessary to passivate the surface of the semiconductor. This was taken through different approaches such as deposition of a so-called interface control layer (ICL) with physical procedures like molecular beam epitaxy (MBE) [1] or thermal evaporation, [7] and chemical treatment of the semiconductor surface in different solutions like $(NH_4)S_x$[8] or gas phase sulfide exposure of the surface.[6]

The deposition of SiN_x:H films is also used to passivate the final surface of bipolar devices based on III–V semiconductors.[9] As in the case of gate dielectric applications, it was a necessary previous treatment of the semiconductor surface to obtain optimum results.

In this article, we present a study of the electrical characteristics of Al/SiN_x:H/InP MIS devices—where the insulator was deposited by ECR—without any treatment of the InP surface prior to SiN_x:H deposition. We show that it is possible to achieve electrical characteristics of the insulator/semiconductor interface that are similar to those reported on devices in which the InP surface was treated by some of the different passivation methods described above.

II. EXPERIMENT

The devices were obtained as follows: we used unintentionally doped n-type InP wafers—5×10^{15} cm^{-3}, ⟨100⟩ orientation. Prior to the insulator deposition, an AuGe/Au (1500 Å 1000 Å) back electrode was thermally evaporated. After this, the wafers were degreased with organic solvents, etched in an H_2IO_3:H_2O (1:10) solution and then immersed for 15 s in HF:H_2O (1:10). Finally, we rinsed them in de-ionized water and dried them in N_2. After the cleaning, we immediately transferred them to the insulator deposition chamber. This was a vacuum chamber—ultimate base pressure 2×10^{-7} Torr—of our own design with an ECR reactor (Astex 4500) attached. Microwave power (100 W), substrate temperature (200 °C) and total pressure (0.6 mTorr) were kept constant in all the experiments. The gases that we used were N_2 and pure SiH_4. The ratio between them, $R=N_2/SiH_4$, was varied from $R=1$ to $R=9$; this allows to change the composition of films—the nitrogen to silicon ratio, N/Si = x—, from $x=0.91$ ($R=1$) to $x=1.49$ ($R=9$). This composition was determined with Auger electron spectroscopy measurements. The deposition time was scaled to obtain a film thickness of 500 Å. Finally, Al dots (1.2×10^{-3} cm^2) were thermally evaporated with a mechanical mask. A post metallization annealing was conducted in Ar atmosphere (300 °C, 20 min).

We characterized the devices by measuring the capacitance–voltage ($C-V$) characteristics—quasistatic (QS) and high frequency (HF) curves—with a Keithley model 82 system. The distribution of interface trap density (D_{it}) was attained on the high-low frequency method.[10] Deep

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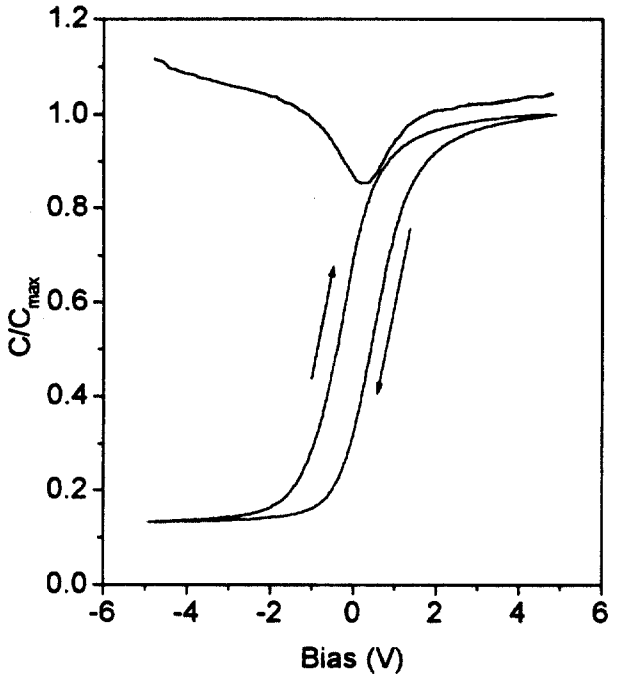

FIG. 1. $C-V$ curves (QS and HF), for an Al/SiN_x:H/InP capacitor in which the composition of the insulator is $x=1.49$.

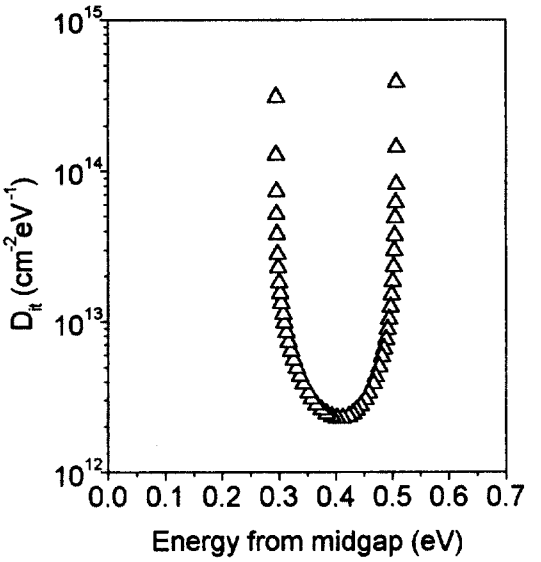

FIG. 2. The interface trap distribution deduced from the data of the structure presented in Fig. 1, as a function of the forbidden gap energy, measured from midgap.

level transient spectroscopy (DLTS) measurements between 100 and 300 K were done by using a 1 MHz Boonton 72B capacitance meter and a Hewlett-Packard (HP) 54501A digital oscilloscope to record the capacitance transients. A Keithley 617 programmable electrometer and a HP214B pulse generator were used to introduce the quiescent bias and the filling pulses, respectively. We also deduced the D_{it} distribution from DLTS measurements with the method described in Ref. 10.

III. RESULTS AND DISCUSSION

In Fig. 1, we present the QS and HF $C-V$ curves of a device in which the insulator composition was $x=1.49$. A well defined QS curve can be observed with a pronounced dip; this means that the insulator/semiconductor interface is of good quality, with low defect content and similar to those described in devices with surface treatments of the different types already described.[6]

In Fig. 2, we present the D_{it} distribution obtained from the data of Fig. 1. The U-shaped form of the curve was observed in all the devices analyzed. This shape is characteristic of $C-V$ measurements and reveals the presence of a minimum in the trap distribution located at 0.42 eV above the midgap, similar to the results of Hashizume *et al.* for MIS capacitors based on InP.[11] The minimum of the trap distribution of Fig. 2 is 2×10^{12} cm^{-2} eV^{-1}. This value and the dependence with the energy are quite similar to the results of Landheer *et al.* [12] for devices in which the InP surface was passivated with a gas phase sulfide exposure before the plasma deposition of the SiN_x:H film. This fact indicates that the insulator/InP interface was very similar in both cases; in ours, the reason is probably that ECR is a remote plasma method, where the substrate is out of the plasma zone and, as a consequence, the damage induced at the InP surface would be minimum in comparison with other conventional direct plasma chemical vapor deposition (CVD) techniques. In a recent study conducted on insulator/InP devices where the insulator was deposited by different plasma CVD techniques, Hashizume[11] showed that the deposition of insulators with a photo-CVD process—a "soft" plasma method—induces small amounts of surface damage on the InP surface, probably due to the low damage character of this technique. Also, the devices that were obtained with this deposition procedure did not show the presence of bulk defects. On the contrary, the devices that were obtained with standard direct plasma CVD techniques exhibited both high values of D_{it} and the presence of bulk defects that were plasma induced. These results reinforce the hypothesis that remote plasma methods like ECR or soft methods like photo-CVD do not induce significant damage in the semiconductor surface and can therefore be used to deposit insulators without the need of previous steps of passivation.

In Fig. 3, we present the D_{it} distribution obtained from DLTS measurements for devices where the composition of the SiN_x:H was comprised between $x=1.1$ and $x=1.49$. Although $C-V$ and DLTS results give D_{it} values of nearly the same order of magnitude, the shape of the distribution turns out to be quite different. $C-V$ results give U-shaped distributions, whereas DLTS results show a different dependence with the energy. These differences have already been observed in devices like SiO_2/InP [11] and SiN_x/InGaAs,[5] and can be accounted for by taking into account that the interface states have not only an energy distribution, but a spatial distribution as well.[13] Hasegawa *et al.*[14] have explained why DLTS measurements tend to underestimate the interface trap density, whereas $C-V$ measurements tend to overestimate it.

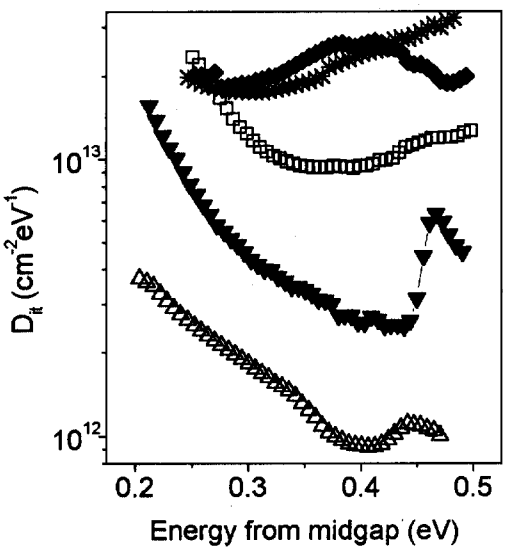

FIG. 3. The interface trap distribution for devices with different insulator compositions, as deduced from DLTS measurements. The SiN_x:H film composition is as follows: (*) $x=1.1$, (♦) $x=1.38$, (□) $x=1.41$, (▼) $x=1.46$, and (△) $x=1.49$.

As we can see in Fig. 3, for the case of the device where the film composition is $x=1.49$, DLTS measurements give values of D_{it} below 2×10^{12} cm^{-2} eV^{-1} in a wide range of energies; this provides the high quality of the interface.

From the results of Fig. 3, we can deduce a strong influence of the insulator composition on the distribution of traps, D_{it}. To assess this influence, in Fig. 4 we present the value of D_{it} at 0.42 eV above the midgap, obtained with DLTS and $C-V$ measurements, as a function of x. Up to a film composition around the stoichiometric value ($x=1.33$), the minimum—obtained from the $C-V$ curves—is continuously decreasing, while the values deduced from DLTS are a slight function of the composition. When the insulator becomes N rich ($x>1.33$), the values measured with the two different techniques closely agree and show a sharp decrease as the films have a higher content of nitrogen. At the highest value of x($x=1.49$), D_{it} minimum is in the low 10^{12} cm^{-2} eV^{-1}, among the best results reported in the literature for this parameter.[6,8,11]

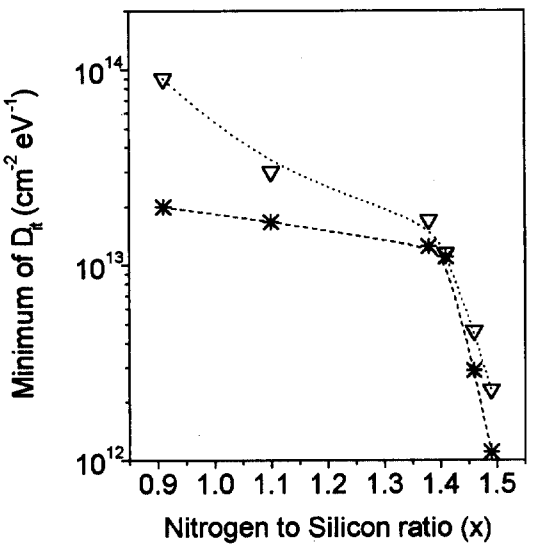

FIG. 4. The minimum value of the interface trap density, as a function of the SiN_x:H insulator composition. Data deduced from $C-V$ measurements (▽), and from DLTS measurements (*).

A commendable explanation of the results can be as follows: when the InP is chemically cleaned or plasma exposed, the surface becomes defective with the volatile element (phosphorous). This leads to a defective surface with P vacancies, V_p, that make the semiconductor unable to be applied in electronic devices where the surface is a key element, like MISFETs. Since the ECR is a remote plasma method, the induced amount of V_p at the InP surface should remain much lower than the number of V_p induced by direct plasma methods. When the insulator is deposited on the top of the InP surface, some intermixing between the film and the semiconductor surface takes place. As a consequence, it seems possible that nitrogen atoms in excess of the insulator move towards the first atomic layers of the semiconductor surface. Once there, nitrogen can fill V_p, taking the place of the formation of a substitutional N_{V_p}. Hence, the devices in which the insulator has the highest nitrogen content would exhibit the lower value of the trap density, since an effective passivation should be expected. The results presented in Figs. 2, 3, and 4 seem to reinforce the explanation shown above. The main consequence is that it may not be necessary to accomplish passivation steps of the semiconductor surface before the insulator deposition itself, as long as it is deposited by the ECR plasma method.

IV. CONCLUSIONS

We have analyzed the influence of the insulator composition on the electrical distribution of interface traps on Al/SiN_x:H/InP capacitors. The analysis of $C-V$ and DLTS characteristics of these structures shows that on devices where the insulator was strongly N rich ($x=1.49$), the interface trap density has a minimum in the range (1–2) $\times10^{12}$ cm^{-2} eV^{-1}. DLTS measurements of this device showed an almost flat distribution of the traps in all the energies analyzed. This points out an effective passivation of the InP surface when the SiN_x:H films are deposited by ECR at conditions that give N-rich films. This passivation is explained as consisting of a substitutional nitrogen located at the V_p, N_{V_p}.

The process here described allows us to obtain SiN_x:H/InP interfaces similar to those reported in devices where the surface was passivated with physical and/or chemical procedures.

ACKNOWLEDGMENT

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[1] D. G. Park, M. Tao, D. Li, A. E. Botchkarev, Z. Fan, Z. Wang, S. N. Mohammed, A. Rockett, J. R. Abelson, and H. Morkoc, J. Vac. Sci. Technol. B **14**, 2674 (1996).
[2] S. Garcia, J. M. Martin, I. Martil, M. Fernandez, and G. Gonzalez Diaz, Philos. Mag. B **73**, 487 (1996).

[3] K. Semo, S. Hayashi, S. Wickramanayaka, and Y. Hatanake, Thin Solid Films **281–282**, 397 (1996).
[4] R. I. Hegde, P. J. Tobin, K. G. Reid, B. Maiti, and S. A. Ajuria, Appl. Phys. Lett. **66**, 2882 (1995).
[5] P. J. M. Permiter and J. G. Swanson, J. Electron. Mater. **25**, 1506 (1996).
[6] A. Kapila, X. Si, and V. Malhotra, Appl. Phys. Lett. **62**, 2259 (1993).
[7] K. Vaccaro, H. M. Dauplaise, A. Davis, S. M. Spaziani, and J. P. Lorenzo, Appl. Phys. Lett. **67**, 527 (1995).
[8] C. S. Sundararaman, P. Milhelich, R. A. Masut, and F. Currie, Appl. Phys. Lett. **64**, 2279 (1994).
[9] A. Kapila, V. Malhotra, L. H. Camnitz, K. L. Seaward, and D. Mars, J. Vac. Sci. Technol. B **13**, 10 (1995).
[10] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).
[11] T. Hashizume, H. Hasegawa, R. Riemenschneider, and H. L. Hartnagel, Jpn. J. Appl. Phys., Part 1 **33**, 727 (1994).
[12] D. Landheer, Z. H. Lu, J. M. Baribeau, L. J. Huang, and W. M. Lau, J. Electron. Mater. **23**, 943 (1994).
[13] L. He, H. Hasegawa, T. Sawada, and H. Ohno, J. Appl. Phys. **63**, 2120 (1988).
[14] H. Hasegawa, M. Akazawa, H. Ishii, A. Uraie, K. Iwadate, and H. Ohno, J. Vac. Sci. Technol. B **8**, 867 (1990).